DISPLAY Elektronik GmbH

DATA SHEET

LCD MODULE

DEM 128064G ADX-PW-N

Product Specification ***Version: 3***

28.09.2017

GENERAL SPECIFICATION

MODULE NO. :

DEM 128064G ADX-PW-N

CUSTOMER P/N:

Version No.	Change Description	Date
0	Original Version	15.06.2017
1	Change the LCD to Transmissive negative and change the OP./ST. Temperature	17.06.2017
2	Correct Module Drawing and Backlight Drawing	14.09.2017
3	Correct Vlcd	28.09.2017

PREPARED BY: GJJ DATE: 28.09.2017

APPROVED BY: MH DATE: 28.09.2017

CONTENTS

1. FUNCTIONS &FEATURES

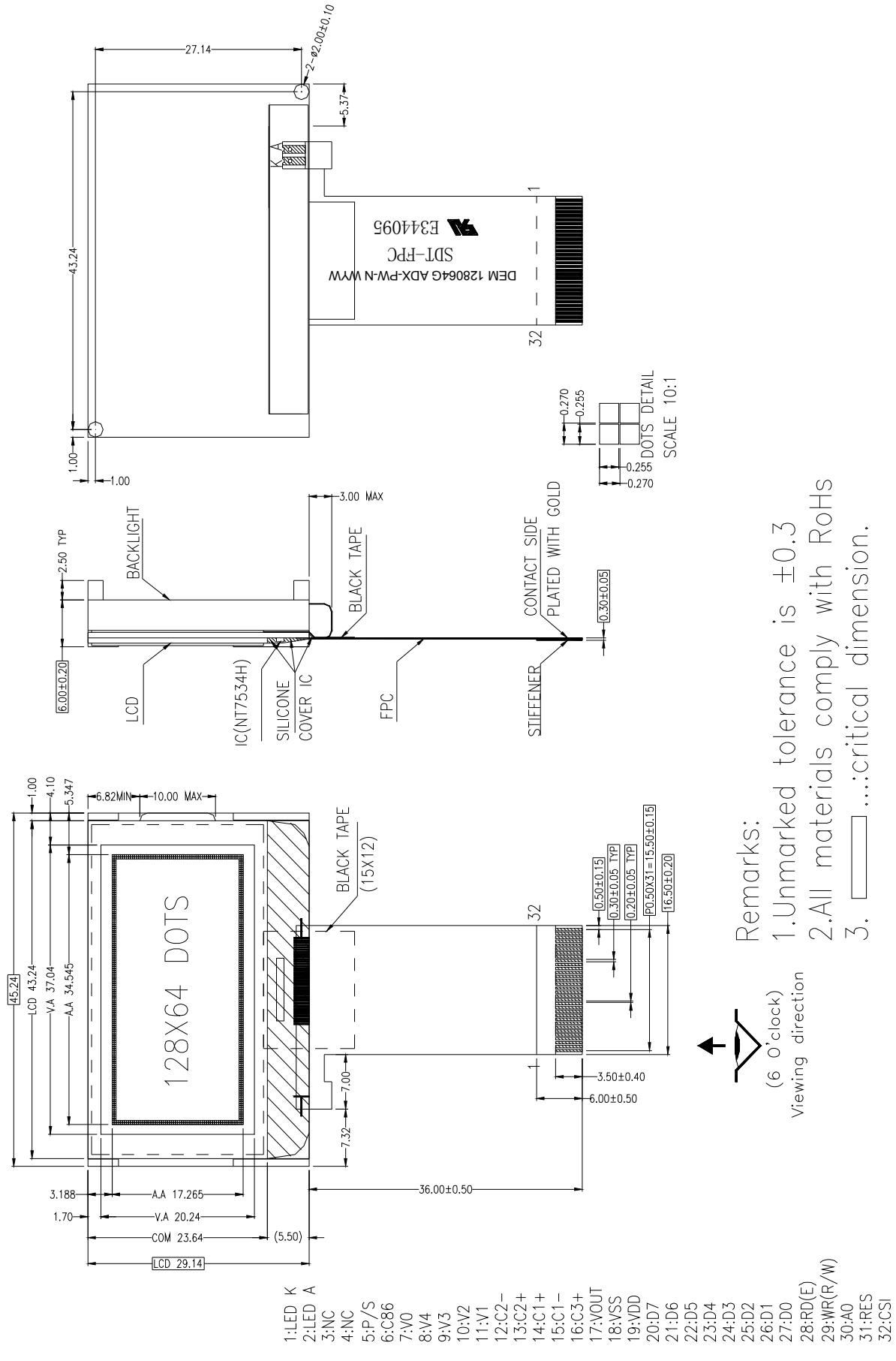
MODULE NAME	LCD Type	Remark
DEM 128064G ADX-PW-N	ASTN Transmissive Negative Mode	

- Viewing Direction : 6 O'clock
- Driving Scheme : 1/ 65 Duty, 1/ 9 Bias
- Power supply : 3.3 Volt (typ.)
- V_{LCD} (V0-Vss) : 11.0 Volt (typ.)
- Display Format : 128 x 64 Dots
- Interface : Parallel & Serial
- LCD Driver : NT7534H (Novatek)
- RoHS Compliant

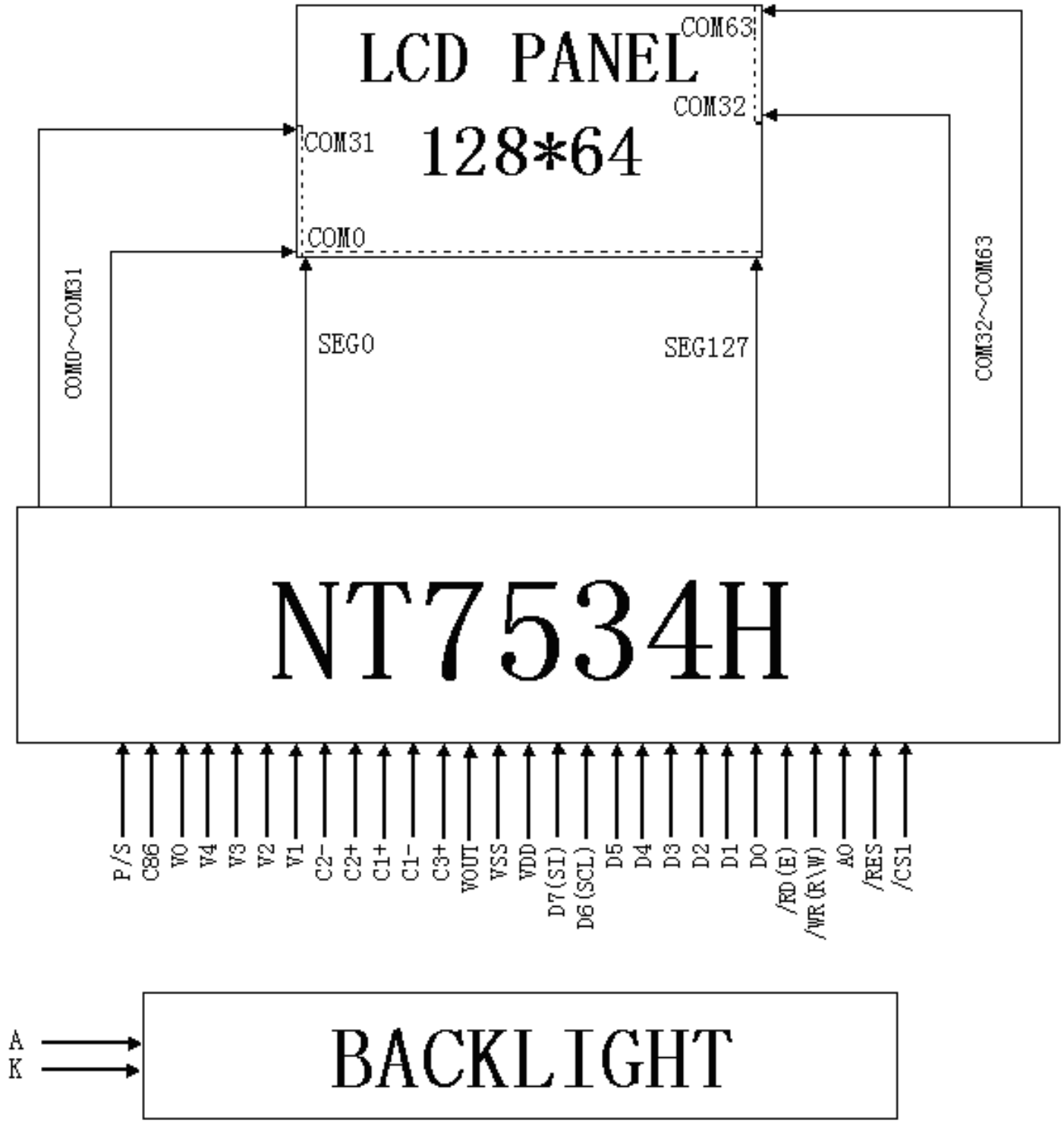
2. MODULE ARTWORK

- Module Size : 45.24 x 29.14 x 6.00 mm (Without FPC)
- Viewing Area : 37.04 x 20.24 mm
- Active Area : 34.545 x 17.265 mm
- Dot Size : 0.255 x 0.255 mm
- Dot Pitch : 0.27 x 0.27 mm
- Dot Gap : 0.015 mm

3. EXTERNAL DIMENSIONS (unit: mm)



4. BLOCK DIAGRAM



5. PIN ASSIGNMENT

<table>
<tr><th>PIN NO.</th><th>Symbol</th><th>Description</th></tr>
<tr><td>1</td><td>K</td><td>Cathode of LED backlight.</td></tr>
<tr><td>2</td><td>A</td><td>Anode of LED backlight</td></tr>
<tr><td>3</td><td>NC</td><td>No connect</td></tr>
<tr><td>4</td><td>NC</td><td>No connect</td></tr>
<tr><td>5</td><td>P/S</td><td>This is the parallel data input/serial data input switch terminal
P/S = “H”: Parallel data input
P/S = “L”: Serial data input
The following applies depending on the P/S status:
<table>
<tr><th>P/S</th><th>Data/command</th><th>Data</th><th>Read/Write</th><th>Serial Clock</th></tr>
<tr><td>“H”</td><td>A0</td><td>D0 to D7</td><td>/RD,/WR</td><td>-</td></tr>
<tr><td>“L”</td><td>A0</td><td>SI(D7)</td><td>Write only</td><td>SCL(D6)</td></tr>
</table>
When P/S = “L”, D0 to D5 are HZ. D0 to D5 may be “H”, “L” or Open. /RD (E) and /WR (R/W) are fixed to either “H” or “L”. With serial data input, RAM display data reading is not supported.</td></tr>
<tr><td>6</td><td>C86</td><td>This is the MPU interface switch terminal
C86 = “H”: 6800 Series MPU interface
C86 = “L”: 8080 Series MPU interface.</td></tr>
<tr><td>7</td><td>V0</td><td rowspan="5">LCD driver supplies voltages. The voltage determined by the LCD cell is impedance-converted by a resistive driver or an operation amplifier for application. Voltages should be according to the following relationship:
V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS2
When the on-chip operating power circuit is on, the following Voltages are supplied to V1 to V4 by the on-chip power circuit.
Voltage selection is performed by the LCD Bias Set command.
<table>
<tr><th>LCD bias</th><th>V1</th><th>V2</th><th>V3</th><th>V4</th></tr>
<tr><td>1/4bias</td><td>3/4 V0</td><td>2/4 V0</td><td>2/4 V0</td><td>1/4 V0</td></tr>
<tr><td>1/5bias</td><td>4/5 V0</td><td>3/5 V0</td><td>2/5 V0</td><td>1/5 V0</td></tr>
<tr><td>1/6bias</td><td>5/6 V0</td><td>4/6 V0</td><td>2/6 V0</td><td>1/6 V0</td></tr>
<tr><td>1/7bias</td><td>6/7 V0</td><td>5/7 V0</td><td>2/7 V0</td><td>1/7 V0</td></tr>
<tr><td>1/8bias</td><td>7/8 V0</td><td>6/8 V0</td><td>2/8 V0</td><td>1/8 V0</td></tr>
<tr><td>1/9bias</td><td>8/9 V0</td><td>7/9 V0</td><td>2/9 V0</td><td>1/9 V0</td></tr>
</table></td></tr>
<tr><td>8</td><td>V4</td></tr>
<tr><td>9</td><td>V3</td></tr>
<tr><td>10</td><td>V2</td></tr>
<tr><td>11</td><td>V1</td></tr>
<tr><td>12</td><td>C2-</td><td>Capacitor 2- pad for internal DC/DC voltage converter</td></tr>
<tr><td>13</td><td>C2+</td><td>Capacitor 2+ pad for internal DC/DC voltage converter</td></tr>
<tr><td>14</td><td>C1+</td><td>Capacitor 1+ pad for internal DC/DC voltage converter</td></tr>
<tr><td>15</td><td>C1-</td><td>Capacitor 1- pad for internal DC/DC voltage converter</td></tr>
<tr><td>16</td><td>C3+</td><td>Capacitor 3+ pad for internal DC/DC voltage converter</td></tr>
<tr><td>17</td><td>VOUT</td><td>DC/DC voltage converter output</td></tr>
<tr><td>18</td><td>VSS</td><td>Ground</td></tr>
<tr><td>19</td><td>VDD</td><td>Power supply input</td></tr>
<tr><td>20</td><td>D7(SI)</td><td rowspan="8">This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected (P/S=“L”), then D7 serves as the serial data input terminal (SI) and D6 serves as the serial clock input terminal (SCL). At this time, D0 to D5 are set to high impedance.
When the chip select is inactive, D0 to D7 are set to high impedance.</td></tr>
<tr><td>21</td><td>D6(SCL)</td></tr>
<tr><td>22</td><td>D5</td></tr>
<tr><td>23</td><td>D4</td></tr>
<tr><td>24</td><td>D3</td></tr>
<tr><td>25</td><td>D2</td></tr>
<tr><td>26</td><td>D1</td></tr>
<tr><td>27</td><td>D0</td></tr>
</table>

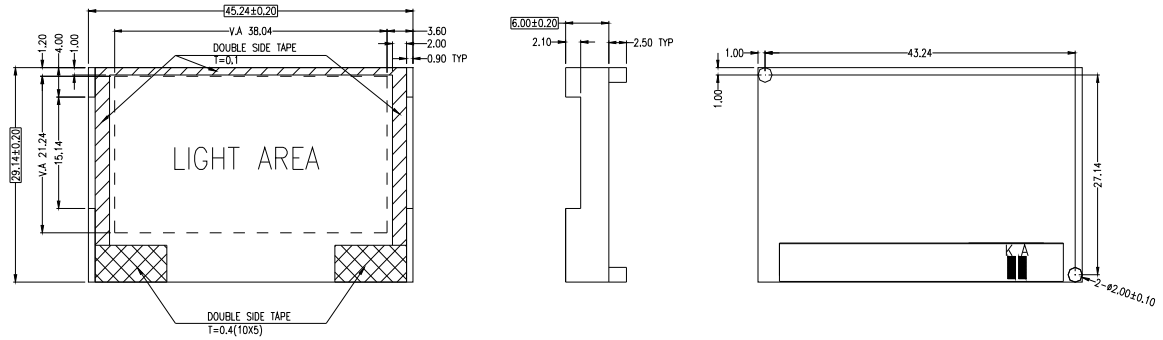
28	/RD(E)	When connected to an 8080 MPU, it is active LOW. This pad is connected to the /RD signal of the 8080MPU, and the NT7534 data bus is in an output status when this signal is “L”. When connected to a 6800 Series MPU, this is active HIGH. This is used as an enable clock input of the 6800 series MPU
29	/WR(R/W)	When connected to an 8080 MPU, this is active LOW. This terminal connects to the 8080 MPU /WR signal. The signals on the data bus are latched at the rising edge of the /WR signal. When connected to a 6800 Series MPU, this is the read/write control signal input terminal. When R/W = “H”: Read When R/W = “L”: Write
30	A0	This is connected to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or a command. A0 = “H”: Indicate that D0 to D7 are display data A0 = “L”: Indicates that D0 to D7 are control data
31	/RES	When /RES is set to “L”, the settings are initialized. The reset operation is performed by the /RES signal level.
32	/CS1	This is the chip select signal. When /CS1=“L” and CS2=“H”, then the chip select becomes active, and data/command I/O is enabled.

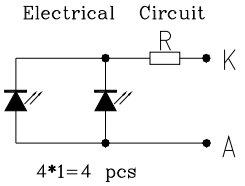
6. BACKLIGHT ELECTRICAL /OPTICAL CHARATERISTICS

Electronics/Optical Specifications: (Color: White)

	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Forward Voltage	V_f	2.9	3.1	3.3	V	
Forward Current	I_f	--	30	40	mA	V_f=3.1V
Power Dissipation	P_d	--	--	0.14	W	V_f=3.1V
Reverse Voltage	V_R	--	--	5	V	--
Reverse Current	I_R	--	--	0.1	mA	V_r=5V
Luminous Intensity	I_V	400	600	--	cd/m^2	V_f=3.1V
Luminous Uniformity	$\triangle I_V$	70	--	--	%	V_f=3.1V
Color Chromaticity	X	0.26	--	0.33	--	I_f=20mA Ta=25° C
	Y	0.26	--	0.33	--	Each chip

	SYMBOL	RATINGS
Operating Temperature	Topr	-20°C to +65°C
	Tsty	-30°C to +75°C





Remarks:
1.Unmarked tolerance is ±0.3
2.All materials comply with RoHs
3. ▭...:critical dimension.
4.COLOR:WHITE
5: LED lifetime 50.000 hours
6: 背光不能印任何供应商标示，编码，日期等图案或字符

7. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	V_{DD}	-0.3	+4.0	V
	Vout	-0.3	+15.0	V
	V0	-0.3	15.0	V
Input Voltage	V_{IN}	-0.3	VDD+0.3	V
Operating Temperature Range	Topr	-30	+80	□
Storage Temperature Range	Tstr	-40	+90	□

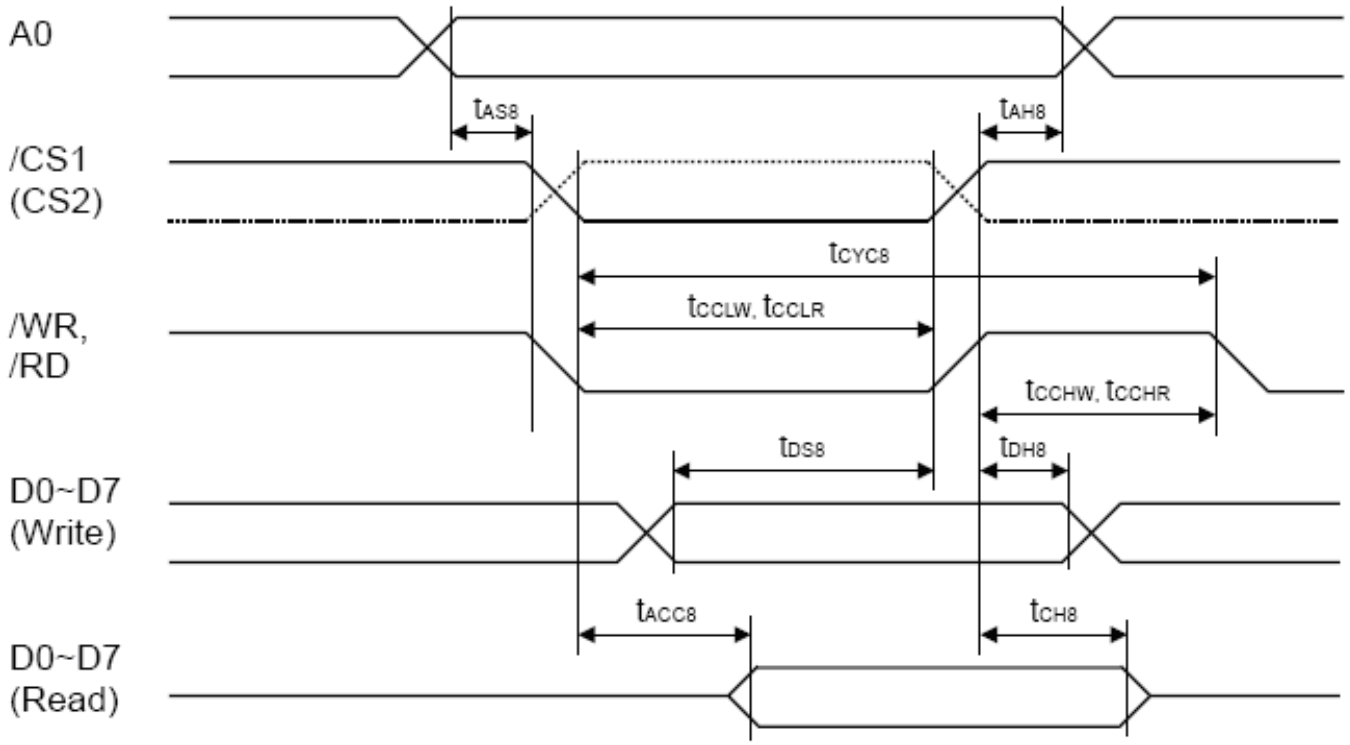
8. ELECTRICAL CHARACTERISTICS

8-1. DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	V_{DD}	3.0	3.3	3.6	V	
LCD Voltage	V_{LCD}	10.7	11.0	11.3	V	V0-V_{SS}
IDD	Current consumption	-	20	35	uA	VDD=3.3V,V0=10.7V, built-in boosting power supply off, display on, Display data=checker and no access Ta=25□
		-	90	160	uA	VDD=3.3V,V0=10.7V,4Xbuilt-in boosting power supply, display on, Display data=checker and no access, Temperature radiant is -0.05%/□, Ta=25□
		-	150	255	uA	VDD=3.3V, V0=10.7V, 4X built-in boosting power supply, display on, Display data=checker and no access, Temperature gradient is -0.05%/□, Ta=25□

8-2. AC Characteristics

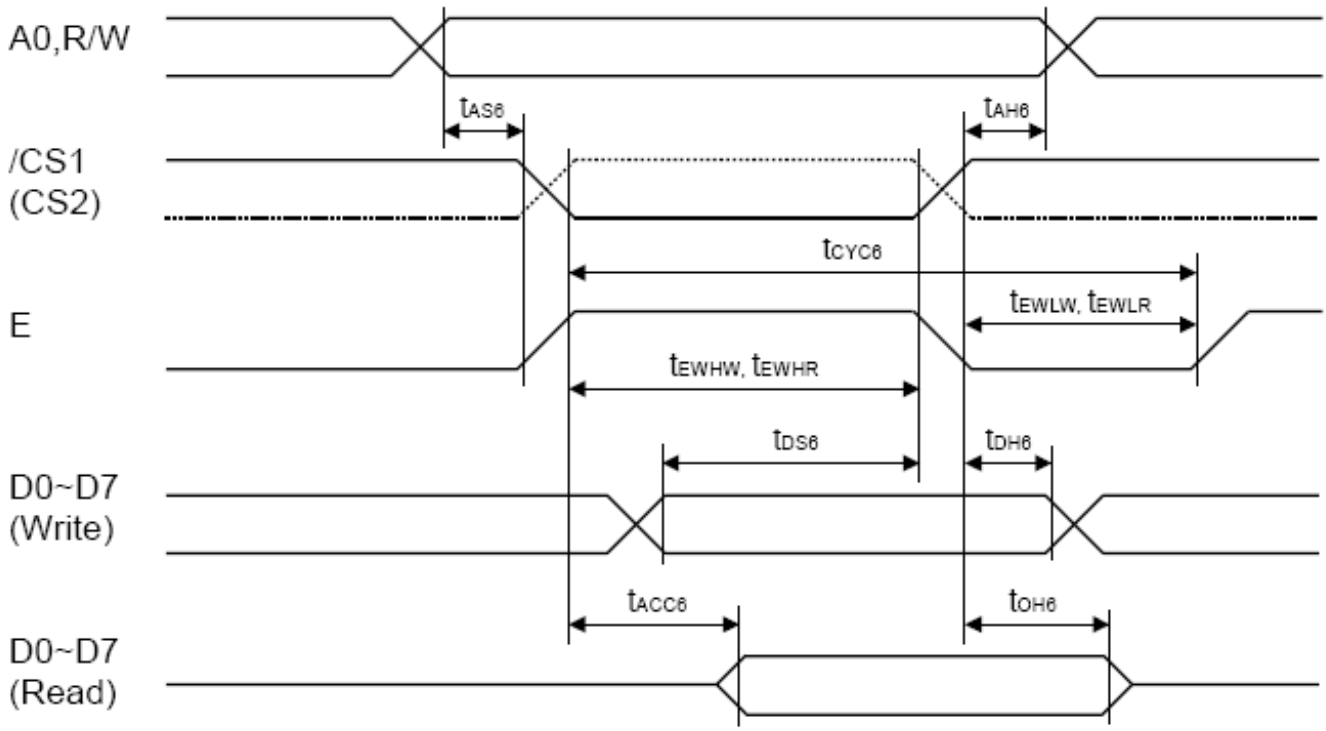
System Buses Read/Write Characteristics (for 8080 Series MPU)



Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
T_{AH8}	Address hold time	0	-	-	ns	A0
T_{AS8}	Address setup time	0	-	-	ns	
t_{CYC8}	System cycle time	240	-	-	ns	
t_{CCLW}	Control low pulse width (write)	90	-	-	ns	/WR
t_{CCLR}	Control low pulse width (read)	120	-	-	ns	/RD
t_{CCHW}	Control high pulse width (write)	100	-	-	ns	/WR
t_{CCHR}	Control high pulse width (read)	60	-	-	ns	/RD
T_{DS8}	Data setup time	40	-	-	ns	D0~D7
T_{DH8}	Data hold time	10	-	-	ns	
t_{ACC8}	/RD access time	-	-	140	ns	D0~D7, CL = 100pF
T_{CH8}	Output disable time	5	-	50	ns	

*1. The input signal rise time and fall time (t_r, t_f) is specified at 15ns or less.
($t_r + t_f$) < (t_{CYC8} - t_{CCLW} - t_{CCHW}) for write, ($t_r + t_f$) < (t_{CYC8} - t_{CCLR} - t_{CCHR}) for read.
*2. All timing is specified using 20% and 80% of VDD as the reference.
*3. t_{CCLW} and t_{CCLR} are specified as the overlap interval when /CS1 is low (CS2 is high) and /WR or /RD is low.

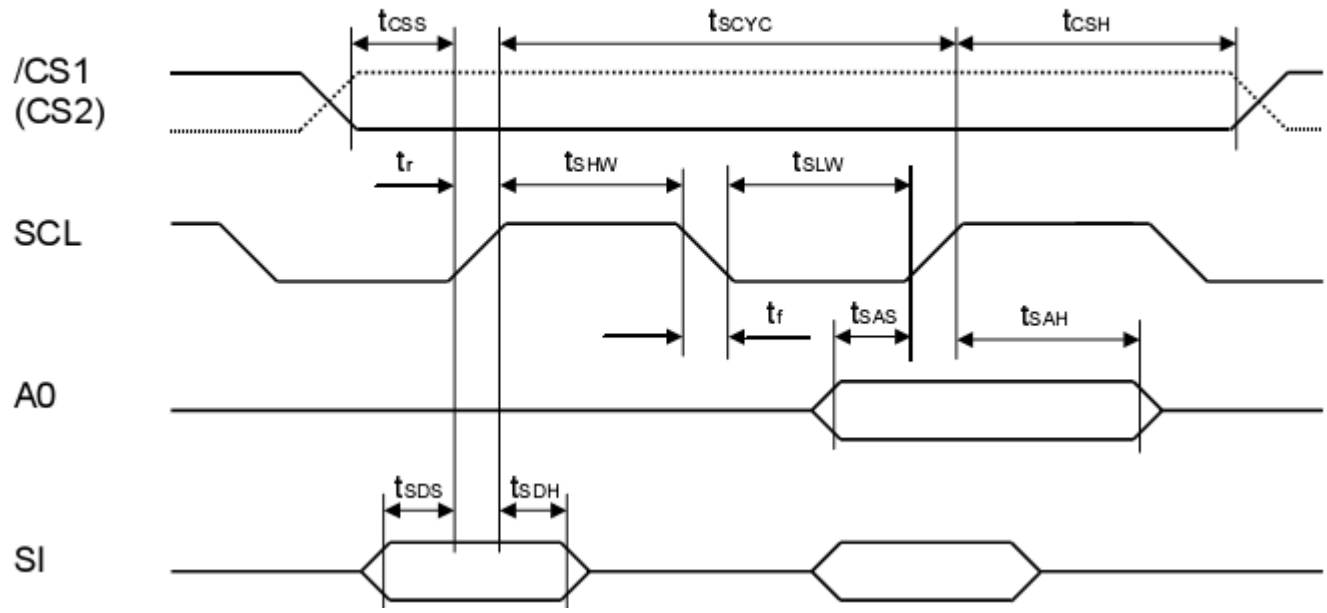
System Buses Read/Write Characteristics (for 6800 Series MPU)



Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{AH6}	Address hold time	0	-	-	ns	A0, R/W
t_{AS6}	Address setup time	0	-	-	ns	
t_{CYC6}	System cycle time	240	-	-	ns	
t_{EWHW}	Control high pulse width (write)	90	-	-	ns	E
t_{EWHR}	Control high pulse width (read)	120	-	-	ns	E
t_{EWLW}	Control low pulse width (write)	100	-	-	ns	E
t_{EWLR}	Control low pulse width (read)	60	-	-	ns	E
t_{DS6}	Data setup time	40	-	-	ns	D0~D7
t_{DH6}	Data hold time	10	-	-	ns	
t_{ACC6}	/RD access time	-	-	140	ns	D0~D7 CL = 100pF
t_{OH6}	Output disable time	5	-	50	ns	

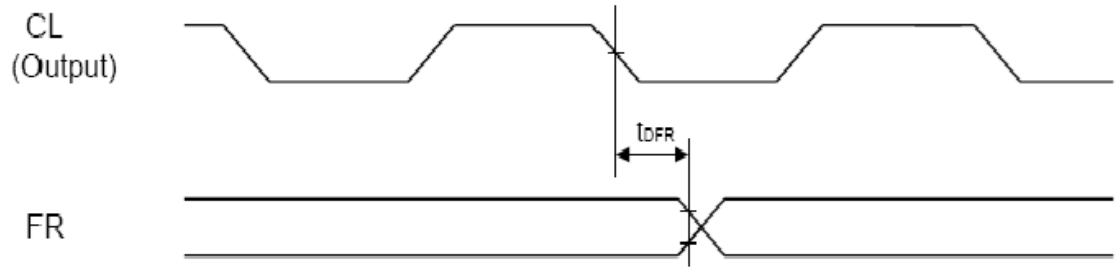
*1. The input signal rise time and fall time (t_r, t_f) is specified at 15ns or less.
($t_r + t_f$) < ($t_{CYC6} - t_{EWLW} - t_{EWHW}$) for write, ($t_r + t_f$) < ($t_{CYC6} - t_{EWLR} - t_{EWHR}$) for read.
*2. All timing is specified using 20% and 80% of VDD as the reference.
*3. t_{EWHW} and t_{EWHR} are specified as the overlap interval when /CS1 is low (CS2 is high) and E is high.

Serial Interface Timing



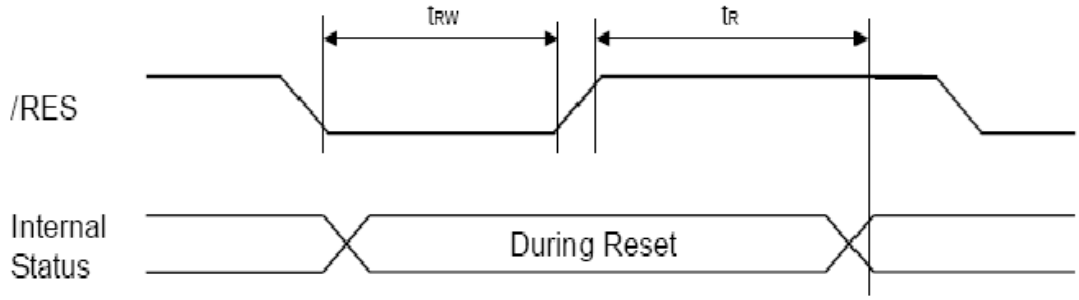
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{SCYC}	Serial clock cycle	120	-	-	ns	SCL
t_{SHW}	Serial clock H pulse width	60	-	-	ns	SCL
t_{SLW}	Serial clock L pulse width	60	-	-	ns	SCL
t_{SAS}	Address setup time	30	-	-	ns	A0
t_{SAH}	Address hold time	20	-	-	ns	A0
t_{SDS}	Data setup time	30	-	-	ns	SI
t_{SDH}	Data hold time	20	-	-	ns	SI
t_{CSS}	Chip select setup time	20	-	-	ns	/CS1, CS2
t_{CSH}	Chip select hold time	40	-	-	ns	/CS1, CS2

Display Control Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{DFR}	FR delay time	-	20	80	ns	CL = 50 pF

Reset Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_R	Reset Time	-	-	1.0	µs	
t_{RW}	Reset low pulse width	10	-	-	µs	/RES

9. INSTRUCTION DESCRIPTION

Command	A0	/RD	/WR	Code									Function
				D7	D6	D5	D4	D3	D2	D1	D0	Hex	
(1)Display OFF	0	1	0	1	0	1	0	1	1	1	0 1	AEh AFh	Turn on LCD panel when high, and turn off when low
(2)Display start line set	0	1	0	0	1	Display start address						40h To 7Fh	Specifies RAM display line for com0
(3)Page address set	0	1	0	1	0	1	1	Page address				B0h To B8h	Set the display data RAM page in page address register
(4)Column address set	0	1	0	0	0	0	1	Higher column address				00h To 18h	Set 4 higher bits and 4 lower bits of column address of display data RAM in register
	0	1	0	0	0	0	0	Lower column address					
(5)Read status	0	0	1	Status				0	0	0	0	XX	Read the status information
(6)Write display data	1	1	0	Write data								XX	Write data in display data RAM
(7)Read display data	1	0	1	Read data								XX	Read data from display data RAM
(8)ADC select	0	1	0	1	0	1	0	0	0	0	0 1	A0h A1h	Set the display data RAM address SEG output correspondence
(9)Normal/Reverse display	0	1	0	1	0	1	0	0	1	1	0 1	A6h A7h	Normal indication when low .but full indication when high
(10)Entire display on/off	0	1	0	1	0	1	0	0	1	0	0 1	A4h A5H	Select normal display (0) or entire display on
(11)LCD bias set	0	1	0	1	0	1	0	0	0	1	0 1	A2h A3h	Sets LCD driving voltage bias ratio
(12)Read –modify-write	0	1	0	1	1	1	0	0	0	0	0	E0h	Increments column address counter during each write
13) End	0	1	0	1	1	1	0	1	1	1	0	EEh	Releases the Read-Modify -Write
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	E2h	Resets internal functions
(15) Common Output Mode Select	0	1	0	1	1	0	1	0 1	*	*	*	C0h to CFh	Select COM output scan direction invalid data
(16) Power Control Set	0	1	0	0	0	1	0	1	Operation Status			28h to 2Fh	Select the power circuit operation mode
17) V0 Voltage Regulator Internal Resistor ratio Set	0	1	0	0	0	1	0	0	Resistor Ratio			20h to 27h	Select internal resistor ratio Rb/Ra mode
(18) Electronic Volume mode Set Electronic Volume Register Set	0	1	0	1	0	0	0	0	0	0	1	81h	
	0	1	0	*	*	Electronic Control Value						XX	Sets the V0 output voltage electronic volume register
(19) Set Static indicator ON/OFF	0	1	0	1	0	1	0	1	1	0	0 1	ACh ADh	Sets static indicator ON/OFF 0: OFF, 1: ON

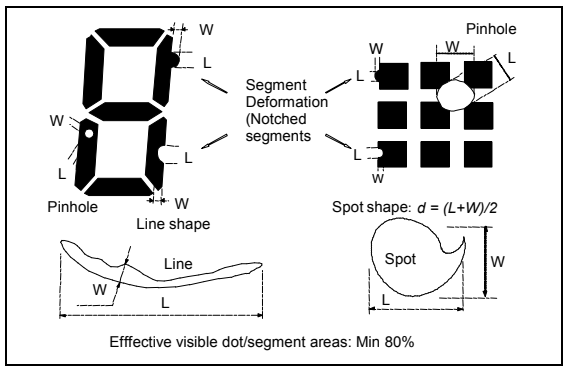
Set Static Indicator Register	0	1	0	*	*	*	*	*	*	Mode		XX	Sets the flash mode
(20) Power Save	0	1	0	-	-	-	-	-	-	-	-	-	Compound command of Display OFF and Entire Display ON
(21) NOP	0	1	0	1	1	1	0	0	0	1	1	E3h	Command for non-operation
(22) Oscillation Frequency Select	0	1	0	1	1	1	0	0	1	0	0 1	E4h E5h	Select the oscillation frequency
(23) Partial Display mode Set	0	1	0	1	0	0	0	0	0	1	0 1	82h 83h	Enter/Release the partial display mode
(24) Partial Display Duty Set	0	1	0	0	0	1	1	0	Duty Ratio			30h 37h	Sets the LCD duty ratio for partial display mode
(25) Partial Display Bias Set	0	1	0	0	0	1	1	1	Bias Ratio			38h 3Fh	Sets the LCD bias ratio for partial display mode
(26) Partial Start Line Set	0	1	0	1	1	0	1	0	0	1	1	D3h	Enter Partial Start Line Set
Partial Start Line Set	0	1	0	1	1	Partial Start Line						XX	Sets the LCD Number of partial display start line
(27) N-Line Inversion Set	0	1	0	1	0	0	0	0	1	0	1	85h	Enter N-Line inversion
Number of Line Set	0	0	*	*	*	*	Number of Line					XX	Sets the number of line used for N-Line inversion
(28) N-Line Inversion Release	0	1	0	1	0	0	0	0	1	0	0	84h	Exit N-Line Inversion
(29) DC/DC Clock Set	0	1	0	1	1	1	0	0	1	1	0	E6h	Set DC/DC Clock Frequency
DC/DC Clock Division Set	0	1	0	1	1	0	0	Clock Division				XX	Set the Division of DC/DC Clock Frequency
(30) Test Command	0	1	0	1	1	1	1	*	*	*	*	F1h to FFh	IC test command. Do not use!
(31) Test Mode Reset	0	1	0	1	1	1	1	0	0	0	0	F0h	Command of test mode reset

NOTE: Do not use any other command, or system malfunction may result

10. QUALITY DESCRIPTION

DEFECT SPECIFICATION:

a: Table for Cosmetic defects
(Note: nc = not counted).
Sizes and number of defects
(Max. Qty)



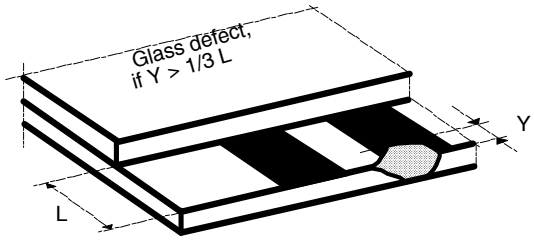
Defect Type	Max. defect size [µm]d or L W	Max. Quantity.
Black or White Spots	d ≤ 100	nc
	100< d ≤ 200	5
Black or White Lines	-- W ≤ 10	nc
	L ≤ 5000 W ≤ 30	3
	L ≤ 2000 W ≤ 50	2
Pinhole	d ≤ 100 100< d ≤ 200	nc1/segment
(Total defects)		(5)
Segment Deformation	W ≤ 100	nc
Bubble (e.g. under pola)	d ≤ 150	nc
	200< d ≤ 400	3
	400< d ≤ 600	1

Examples/Shapes

b: Glass defects

b1:Glass defects at contact ledge

b2:Glass chipping in other areas shall not be in conflict



with the product's function.

11. ACCEPT QUALITY LEVEL (AQL).

11.1. AQL standard value: Critical defect =0.1; Major defect=0.65; Minor defect =2.5.

11.2. Inspection Standard: MIL-STD-105E Table Normal Inspection Single Sampling Level □.

12. RELIABILITY TEST CONDITION

Operating life time: 50,000 hours (at room temperature without direct irradiation of sunlight)
Reliability characteristics shall meet following requirements.

Test Item	Test Condition
High temperature storage	+90℃ x 96HR
Low temperature storage	-40℃ x 96HR
High temperature operation	+80℃ x 96HR
Low temperature operation	-30℃ x 96HR
High temperature, High humidity	+60℃ x 90%RH x 96HR
Thermal shock	-30□ x 30min → 25□ x 10s → +80□ x 30min x 5 Cycles
Vibration test	Frequency x Swing x Time 40Hz x 4mm x 4hrs
Drop test	Height x no. of drop 1.0m x 6 drops

13. LCD MODULES HANDLING PRECAUTIONS

- The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.
- If the display panel is damaged and the liquid crystal substance inside it leaks out, do not get any in your mouth. If the substance come into contact with your skin or clothes promptly wash it off using soap and water.
- Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.
- The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarize carefully.
- To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

  -Be sure to ground the body when handling the LCD module.

  -Tools required for assembly, such as soldering irons, must be properly grounded.

  -To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

  -The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.
- Storage precautions

  When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps. Keep the modules in bags designed to prevent static electricity charging under low temperature / normal humidity conditions (avoid high temperature / high humidity and low temperatures below -20□). Whenever possible, the LCD modules should be stored in the same conditions in which they were shipped from our company.

14. OTHERS

- Liquid crystals solidify at low temperature (below the storage temperature range) leading to defective orientation of liquid crystal or the generation of air bubbles (black or white). Air bubbles may also be generated if the module is subjected to a strong shock at a low temperature.
- If the LCD modules have been operating for a long time showing the same display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. Abnormal operating status can be resumed to be normal condition by suspending use for some time. It should be noted that this phenomena does not adversely affect performance reliability.
- To minimize the performance degradation of the LCD modules resulting from caused by static electricity, etc. exercise care to avoid holding the following sections when handling the modules:
  - Exposed area of the printed circuit board
  - Terminal electrode sections.